REMARKS/ARGUMENTS

By this paper, Applicant responds to the Office Action of March 24, 2005 and respectfully requests reconsideration of the application. The shortened statutory period runs through June 24, 2005. Accordingly, this response is timely.

Claims 1-43 are now pending, a total of 43 claims. Claims 1, 9, 13, 16, 22, 24, 34, 36 are independent. Claims 1-33 are allowed, and 40-43 are indicated as reciting allowable subject matter.

I. Claims 34 and 36

Claim 36 recites as follows:

> 36. A computer, comprising:
>
> hardware designed to recognize a condition rising during execution of an instruction on a computer, in which the instruction is to affect the execution of a second instruction;
>
> hardware and/or software designed to respond to the recognizing by setting a processor of the computer into single-step mode; and
>
> hardware and software designed to respond to execution of the second instruction by setting the computer out of single-step mode.

A. Claim 36 is Patentable on the Merits

As noted below, the Office Action is too vague and incomplete to state a rejection, let alone permit a direct response. Nonetheless, in an effort to advance prosecution, Applicant offers the following observations.

Pages 195-197 of the specification illustrate several instances where a later instruction executes differently because of a condition detected in an earlier instruction. For example, because of an anomaly in the definition of the Intel X86 architecture, in some cases a MOV instruction is defined to not fully complete by the immediately-following instruction boundary. Instead, MOV has side effects that wait to complete until the boundary following the next instruction. Similarly, in some cases, the STI instruction is defined to not take effect at the immediately following instruction boundary, but in the instruction boundary following the next instruction. The need to hold these effects in "suspended animation," instead of architecturally committing them at the first instruction boundary like every other side-effect of every other

instruction, is a significant disruption to an otherwise "clean" design. The specification teaches techniques implemented in hardware and software to implement those "delayed effects."

Claim 36 recites the novel elements of the specification's examples. During execution of a first instruction, the processor recognizes that a condition has occurred that should affect execution of a second instruction – that is, the processor recognizes that the effect of the first instruction is not self-contained within the first instruction, but is to affect the way the second instruction executes. Claim 36 recites that, in order to achieve the required cross-instruction effect, the processor is put into single-step mode. The specification teaches that the processor may hand off responsibility to emulator software to control instruction execution. When the second instruction completes, then emulator software can ensure that the delayed effect of the first instruction is architecturally commited at the right time. Then claim 36 resumes: once the second instruction is complete (including the cross-instruction effect of the first instruction), then "the processor [is set] out of single-step mode" so it can resume normal execution.

In contrast, the indicated portion of Alpert '679 (col. 2, lines 17-19) only discusses conventional instruction behavior, in which the effect of the instruction is fully self-contained, and fully committed by the immediately-following instruction boundary. For example:

> When enabled, a single step trap occurs after the execution of the current instruction.

This portion of Alpert '679 discusses none of the anomalous cross-instruction execution effects of the Intel architecture, and thus raises no need to "recognize a condition in which an instruction is to affect the execution of a second instruction," let alone responding to that condition in the manner recited in claim 36.

Claim 34 recites similar language, and is patentable for similar reasons.

B. Procedurally, the Office Action is Too Incomplete to Raise any Rejection

The Office Action is too unclear to constitute a rejection. It compares claim 32 in "one bite" to nearly two columns of text (col. 1, lines 13 to col. 2, line 63), supplemented by unspecified "well known" prior art. The Office Action makes no element-by-element comparison of any claim term to any particular element of any reference. Applicant is left to guess: What instructions of these two columns correspond to each of the two instructions of the

claim? What in these two columns corresponds to the "condition" of the claim? Without the "explanation of pertinence" required by 37 C.F.R. § 1.104(c)(2), Applicant is unable to determine the Examiner's thoughts or respond. Without that explanation, no rejection exists.

Second, the Office Action asserts that is "well known to include conditions that affect another instruction." The Office Action misquotes the claim – the claim recites an effect on "execution." Different data, such as suggested in the Office Action, might affect the result of a later instruction, but almost never the fundamental "execution." For example, an ADD instruction always executes as an addition, never varying its execution (as opposed to its data-dependent result) based on a preceding or following instruction. Also, such behaviors are hardly "well known," they are extremely uncommon. Almost all instructions are self-contained – only rarely does one see in a hardware manual a statement that an instruction varies its "execution" based on a different instruction.

Third, 37 C.F.R. § 1.104(d)(2) requires that when an Office Action "relies on facts within the personal knowledge of an employee ... the data shall be as specific as possible." The Action's assertion of "well known" conditions does not designate any specific "condition" or factual basis to believe the assertion is "well known." Such a vague statement makes it impossible for an applicant to respond – no rejection exists. If any rejection is raised in any future Action, Applicant "calls for" a specific reference or an affidavit, pursuant to § 1.104(d)(2).

Fourth, the Office Action errs by disassembling the claim into disconnected bits, and comparing the bits to unrelated parts of the reference and to unidentified "well known" prior art. The Office Action makes no showing that the prior art teaches the claim elements arranged and interrelated as recited. For example, the Office Action points to no single instruction in Alpert that corresponds to all instances of the "second instruction" recited in claim 34. Instead, the Office Action apparently compares the first instance of "second instruction" to an unspecified "well known" instruction, and the second instance to a different (but still unspecified) instruction in Alpert '679. No rejection exists.

Fifth, the Office Action treats a number of the dependent claims as though they were free standing claims, unrelated to the independent claims from which they depend, and treats other claims with insufficient care. For example, the Office Action notes that claim 39 recites the

words "stack" and "register," but ignores the word "segment," makes no effort to deal with the term of art "stack segment register," and makes not attempt to show that the portions of Alpert '679 indicated for claim 39 interrelate to the portions indicated for claim 36 (on which claim 39 depends) in the manner recited in claim 39. Many of the remaining claims are given similar short shrift, with no indication of which particular circuits in Alpert '679 correspond to which portions of the claims.

Such piecemeal examination is discouraged by 37 C.F.R. § 1.105 and MPEP § 707.07(g). It is requested that any future Office Action indicate the allowability of any claim that recites a limitation against which no prior art is cited.

II. Conclusion

In view of these remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. The Examiner is urged to telephone Applicant's undersigned counsel at the number noted below if it will advance the prosecution of this application, or with any suggestion to resolve any condition that would impede allowance. In the event that any extension of time is required, Applicant petitions for that extension of time required to make this response timely. Kindly charge any additional fee, or credit any surplus, to Deposit Account No. 23-2405, Order No. 114596-29-0125BS.

Respectfully submitted,

WILLKIE FARR & GALLAGHER LLP

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By: _____

David E. Boundy
Registration No. 36,161

WILLKIE FARR & GALLAGHER LLP
787 Seventh Ave.
New York, New York 10019
(212) 728-8000
(212) 728-8111 Fax